Carrier transport and sensitivity issues in heterojunction with intrinsic thin layer solar cells on N-type crystalline silicon: A computer simulation study

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Heterojunction with intrinsic thin layer or "HIT" solar cells are considered favorable for large-scale manufacturing of solar modules, as they combine the high efficiency of crystalline silicon (c-Si) solar cells, with the low cost of amorphous silicon technology. In this article, based on experimental data published by Sanyo, we simulate the performance of a series of HIT cells on N-type crystalline silicon substrates with hydrogenated amorphous silicon (a-Si:H) emitter layers, to gain insight into carrier transport and the general functioning of these devices. Both single and double HIT structures are modeled, beginning with the initial Sanyo cells having low open circuit voltages but high fill factors, right up to double HIT cells exhibiting record values for both parameters. The one-dimensional numerical modeling program "Amorphous Semiconductor Device Modeling Program" has been used for this purpose. We show that the simulations can correctly reproduce the electrical characteristics and temperature dependence for a set of devices with varying I-layer thickness. Under standard AM1.5 illumination, we show that the transport is dominated by the diffusion mechanism, similar to conventional P/N homojunction solar cells, and tunneling is not required to describe the performance of state-of-the art devices. Also modeling has been used to study the sensitivity of N-c-Si HIT solar cell performance to various parameters. We find that the solar cell output is particularly sensitive to the defect states on the surface of the c-Si wafer facing the emitter, to the indium tin oxide/P-a-Si:H front contact barrier height and to the band gap and activation energy of the P-a-Si:H emitter, while the I-a-Si:H layer is necessary to achieve both high V_{oc} and fill factor, as it passivates the defects on the surface of the c-Si wafer. Finally, we describe in detail for most parameters how they affect current transport and cell properties.
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I. INTRODUCTION

Heterojunction with intrinsic thin layer or "HIT" solar cells, which combine the high stable efficiency of crystalline silicon (c-Si) cells with the low temperature deposition technology of hydrogenated amorphous silicon (a-Si:H) to produce both the emitter and back surface field (BSF) layers, are gaining in popularity as a low cost alternative to c-Si solar cells. In fact, Sanyo has attained record conversion efficiencies of 22.3%,[1] with 21.85% (Ref. 2) for a practical size of 100.4 cm^2 and 17.3% module efficiency[2] in HIT structures on N-type c-Si substrates, leading to industrial production already in 2003. Sanyo has focused on P-a-Si:H/N-c-Si HIT structures,[1–6] while European and U.S. groups have studied both P-a-Si:H/N-c-Si and N-a-Si:H/P-c-Si, structures,[7–10,30] with the maximum efficiency on P-type substrates reaching between 17% and 18%.[7,10,30] Recent studies have focused on the optimization of these devices in order to maximize the conversion efficiency. In HIT cells, in addition to the usual surface texturing techniques,[11] increases in efficiency have been obtained by optimized c-Si surface cleaning process, high quality and low damage intrinsic a-Si:H deposition technology, and in general by attaining good amorphous-crystalline (a-c) heterointerfaces and passivation of defects on the surface of the c-Si wafer, e.g., Ref. 2. Computer modeling of HIT structures has been carried out, not only to understand carrier transport in these structures,[12–16] but also to assess which HIT structure—whether on N-type or P-type c-Si substrate—is capable of attaining the higher efficiency.[13,14,17]

In this article, we have used the detailed numerical electrical-optical model, Amorphous Semiconductor Device Modeling Program (ASDMP),[18,19] to trace the development of the Sanyo cells, beginning with their initial front HIT (with a heterojunction (HJ) only on the emitter side, and a conventional BSF layer, that is part of the c-Si wafer itself) solar cells, having rather low values of the open-circuit voltages (V_{oc}).[4] Their initial double HIT cells (where both the

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emitter and BSF layers are amorphous, and hence have HJs at either end of the c-Si wafer) also suffered from low V_{oc}.[5] However, in spite of this drawback, the efficiency (η) was remarkably high, due to very high values of the fill factor (FF) and short-circuit current density (J_{sc}), the latter mainly due to improved light-trapping induced by a textured c-Si surface. In recent editions of their cells.[1,2,6] however, record values of both the V_{oc} and FF have been achieved and by simulating Sanyo cells at different stages of development in this article; we have tried to understand the reasons. We also know that Fuhs *et al.*,[20] as early as in 1974, had already tried to combine c-Si and a-Si:H technology to produce HJ solar cells. However, they could not attain satisfactory cell efficiencies. It was only when the Sanyo group introduced an intrinsic a-Si:H (I-a-Si:H) layer on the surface of the c-Si wafer, before depositing the emitter P-a-Si:H, in their innovative artificially constructed junction-HIT layer (ACJ-HIT, now shortened to HIT)[3–5] solar cells, that efficiencies comparable to c-Si cells could be achieved. In this article, therefore, we have also laid special emphasis on understanding the role of this I-a-Si:H layer. Finally, the sensitivity of the solar cell output of N-c-Si HIT cells to various material and device properties has been studied.

Modeling of HIT structures on N-type c-Si substrate has already been carried out by a few groups,[12–14,16] one of which[12] has tried to establish that tunneling of holes across the potential barrier due to the large valence band discontinuity, which may explain the high FF in these structures. The second group,[13,14] however, has ignored tunneling and has shown that the HIT cells on N-type c-Si substrates are expected to have higher values of both J_{sc} and V_{oc}, but lower values of the FF, relative to HIT cells on P-type c-Si substrates. A third group[16] has argued that indium tin oxide (ITO), the standard transparent conducting oxide (TCO) used as the front contact in HIT cells, is an N-type semiconductor, and that therefore this structure is essentially a N (ITO)/P-a-Si:H/N-c-Si structure, which should produce poor performance, with a particularly low FF. According to this group, the fact that the latter is quite high in HIT cells implies that tunneling of carriers is an important transport mechanism in these structure. Experimentally Taguchi *et al.*[6] have also suggested that multistep tunneling is the dominant transport mechanism across the junction interfaces in the voltage range $0.1\ \mathrm{V} < \mathrm{V} < 0.4\ \mathrm{V}$, i.e., for low bias, the possibility of which had already been suggested by several authors.[21–24] In this article, we will use our simulations of experimental results, with model ASDMP, which does not include tunneling, to also comment on the dominant mechanism of carrier transport in N-type HIT structure solar cells.

II. SIMULATION MODEL

The ASDMP,[18,19] which was originally conceived to model amorphous silicon based devices and later extended to HIT cells,[15] has been used in all calculations in this article. This one-dimensional numerical modeling program solves the Poisson's equation and the two carrier continuity equations under steady state conditions for the given device structure. It yields the dark and illuminated current density-voltage (J-V) characteristics and the quantum efficiency. The electrical part of this program is described in Refs. 25 and 26. The expressions for the free and trapped charges, the recombination term, the boundary conditions, and the solution technique in this program are similar to the AMPS computer program.[27] Tunneling, either "direct" or "multistep," has not yet been incorporated into ASDMP, although an auxiliary program for calculating the direct tunneling probability and the resultant direct tunneling current density has been developed.[28] This program is used later in this article to estimate the probability of direct tunneling of holes to the front contact and the resultant hole current density for valence band offsets between amorphous and crystalline silicon where such tunneling can be appreciable.

The gap state model for the amorphous layers consists of the tail states and two Gaussian distribution functions to simulate the deep dangling bond states. This same density of states (DOS) model can be used for c-Si as well, with the tail states absent, and the lifetime of the minority carriers may be estimated using the formula

$$\tau_p \approx \frac{p - p_0}{R} \tag{1}$$

where τ_p, p, and p_0 are the hole lifetime, the free hole density under the given experimental conditions (in this case under 100 mW cm^{-2} of AM1.5 light), and the hole density at thermodynamic equilibrium respectively, while R is the recombination rate in the N-c-Si wafer. The lifetime, calculated in this manner, is in general, a function of position in the device; however, over a large region inside the N-c-Si wafer, away from the edges, it is constant and it is this value that is taken to be the minority carrier lifetime in the wafer. van Cleef *et al.*[12] and Kanevce *et al.*[16] have also used the DOS model to simulate the c-Si parts of their HIT cells.

The generation term in the continuity equations has been calculated using a semiempirical model[29] that has been integrated into ASDMP.[18,19] Both specular interference effects and diffused reflectances and transmittances due to interface roughness can be taken into account. The complex refractive indices for each layer of the structure are required as input and have been measured in house by spectroscopic ellipsometry. In all cases studied in this article, experimentally or by modeling, light enters through the ITO/P-a-Si:H window, and this junction between the ITO and P-layers is taken as $x=0$ on the position scale in the modeling calculations and referred to as the front contact. Voltage is also applied at $x=0$. The BSF(N^{++})/ITO contact at the back of the c-Si wafer is taken as $x=L$ on the position scale, where L is the total thickness of all the semiconductor layers of the device. This contact, to be referred to as the back contact, is assumed to be at ground potential.

III. SIMULATION OF EXPERIMENTAL RESULTS

Simulation of a range of experimental results on HIT cells developed by the Sanyo group and available in the literature[2,4–6] has been undertaken to extract typical parameters that characterize state-of-the-art HIT cells on N-type crystalline silicon substrates, as well as to gain an insight

TABLE I. Comparison between measured (E) and modeled (M) solar cell output of front (F) and double (D) N-c-Si HIT cells with textured TCO front contact, developed by Sanyo over the years [2,4,5]. The exponents on "E" give the related references.

HIT		N_{ss} (cm^{-2}) Front	N_{ss} (cm^{-2}) Rear	τ (ms)	V_{oc} (mV)	J_{sc} (mA cm^{-2})	FF	η (%)
F	E^4	⋯	⋯	⋯	638	37.90	0.775	18.74
	M	4×10^{11}	⋯	0.23	643	37.89	0.775	18.88
D-I	E^5	⋯	⋯	⋯	644	39.40	0.790	20.05
	M	4×10^{11}	10^{11}	0.5	658	39.03	0.783	20.11
D-II	E^2	⋯	⋯	1.20	718	38.52	0.790	21.85
	M	10^{11}	10^{11}	2.00	713	38.60	0.797	21.93

into carrier transport and the general functioning of these cells. Both "front" HIT cells having an a-c HJ on the emitter side,[4] where the light enters and "double" HIT cells having HJs on both ends of the c-Si wafer[2,5,6] have been simulated. The cells have the following structure: ITO/P-a-Si:H/I-a-Si:H/textured N-c-Si/N-c-Si BSF/metal (front HIT)[4] and ITO/P-a-Si:H/I-a-Si:H/textured N-c-Si/I-a-Si:H/N^{++}-a-Si:H/metal (double HIT).[2,5,6] In Ref. 6, after depositing the undoped and doped a-Si:H layers on both ends of the c-Si wafer, ITO films were sputtered on both sides as the TCO layers, followed by screen-printed silver grid electrodes. Article Refs. 4, 5, and 2, trace the development of the Sanyo HIT cells on N-type c-Si over the years, from the initial cells[4,5] having low open-circuit voltages, but quite high FFs right up to more recent cells, e.g., Refs. 2 and 6 having record values of both V_{oc} and FF. Simulation of these cells[4,5,2] gives us an insight into the parameters that play a crucial role in improving HIT cell performance. On the other hand, the article by Taguchi *et al.*[6] gives the temperature dependence of the dark current density-voltage characteristics and the solar cell output parameters as a function of the thickness of the intrinsic amorphous layer sandwiched between the emitter P-a-Si:H and the main absorber N-c-Si. A study of the temperature dependence of the dark J-V characteristics is particularly important to understand the carrier transport mechanism in these devices. The parameters extracted by such modeling will be used in the following sections to calculate the sensitivity of the solar cell performance to various controlling factors.

In Table I, we compare our simulation results to the experimental results of various HIT cells on N-type c-Si substrates.[2,4,5] Modeling indicates that improvements in V_{oc} could be brought about (a) by going from a front HIT to a double HIT structure, (b) by decreasing the defects (N_{ss}) on the surface of the crystalline silicon wafer, and (c) by improving the lifetime of the minority carriers in crystalline silicon. These modeling results show that it is by decreasing N_{ss} on the front surface of the c-Si wafer, that the large increase in V_{oc} could be achieved without any fall in FF, with a high lifetime of the minority carriers in c-Si playing a supporting role.

We next used ASDMP to simulate the experimental results of Taguchi *et al.*[6] These authors have concentrated on the temperature dependence of the dark and light J-V characteristics of their N-c-Si HIT cells and on the effect of vary-

TABLE II. Modeling of the experimental output parameters of HIT structure solar cells on N-type c-Si wafer (Ref. 6), having different thickness of the I-a-Si:H layer on the emitter side. μ_n (μ_p) is the band microscopic electron (hole) mobility in the P- and I-a-Si:H layers. N_{ss} (DL) is the defect density on that surface of the c-Si wafer that faces the emitter. The quantities marked with "*" are the calculated values of FF and efficiency taking into account the series resistance of the contacts (2.8 mΩ) (Ref. 6). The addition of the series resistance did not modify V_{oc} and J_{sc}.

Cell name	μ_n (μ_p) (cm^2/V s)	I-a-Si:H thickness (nm)	N_{ss} (DL) (cm^{-2})		J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	Efficiency (%)
Half	30 (6)	1.5	4×10^{11}	Expt.	37.4	0.699	0.776	20.3
				Model	37.2	0.702	0.803	21.0
							0.775*	20.2*
Normal	25 (5)	3.0	1.5×10^{11}	Expt.	37.2	0.711	0.773	20.4
				Model	37.0	0.712	0.799	21.0
							0.774*	20.4*
Double	15 (3)	6.0	10^{10}	Expt.	36.5	0.718	0.747	19.6
				Model	36.7	0.717	0.766	20.2
							0.747*	19.7*
Triple	15 (3)	9.0	10^{10}	Expt.	36.4	0.715	0.717	18.7
				Model	36.6	0.714	0.750	19.6
							0.718*	18.8*

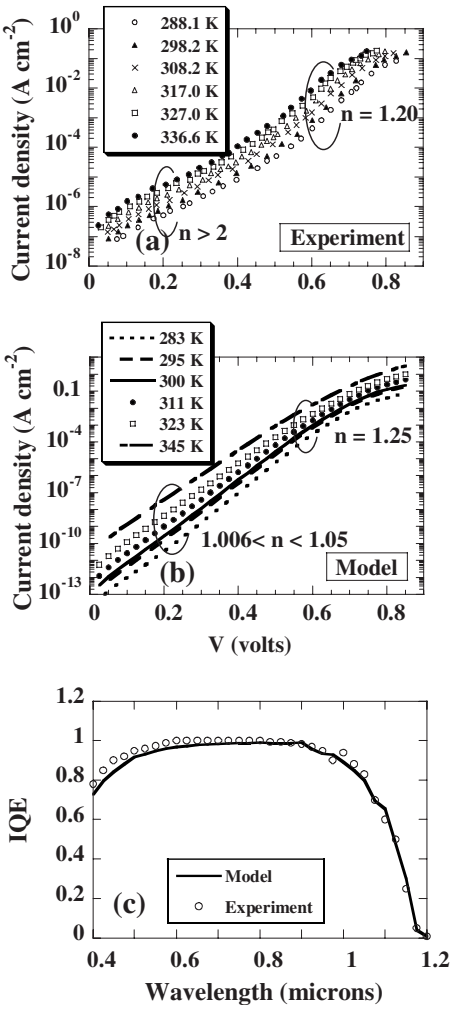

FIG. 1. (a) Experimental (Ref. 6) and (b) simulated dark J-V characteristics of the cell with normal thickness I-a-Si:H layer at the P-a-Si:H/N-c-Si interface at various temperatures, and (c) the IQE of the same cell under AM1.5 illumination and 0 V compared to the experimental IQE of a typical Sanyo cell (Ref. 2).

ing the thickness of the intrinsic amorphous silicon layer at the P-amorphous emitter/N-c-Si HJ. The terminology "normal" has been used by Taguchi *et al.*[6] to represent the thickness of the I-a-Si:H buffer layer (front) in the cell that yields the highest efficiency (Table II). Our simulations point to a thickness of about 3 nm for this layer. The I-a-Si:H buffer layers (front) in the cells named "half," "double," and "triple" by Taguchi *et al.*[6] have therefore been assigned thicknesses of 1.5, 6, and 9 nm, respectively, in the modeling calculations. In all the cases, this layer is assumed to have the same dangling bond density and capture cross-sections. The results of our simulation of the experimental light J-V characteristics[6] as a function of the I-a-Si:H layer thickness are given in Table II and the input parameters extracted by such modeling and also of the dark J-V characteristics [Figs. 1(a) and 1(b)] and typical internal quantum efficiencies of Sanyo N-c-Si HIT cells [Fig. 1(c)—Maruyama *et al.*[2]] are given in Table III. Since modeling does not consider the resistance of the contacts, the modeling results had to be modified by taking into account the series resistance of the contacts, given in the article by Taguchi *et al.*[6] The addition of the series resistance did not modify V_{oc} and J_{sc} but allowed to perfectly match the experimental FF and therefore the efficiency of the Sanyo HIT solar cells.[6] In Table II, we show the solar cell output parameters as obtained directly by modeling, without resistive losses (which gives an upper limit for the FF and therefore the efficiency) and the values of the FF and efficiency after taking into account the constant series resistance (marked by "*"). This resistance, taking into account the resistive losses in the TCO, the silver grid and the contacts, was estimated by Taguchi *et al.*[6] to be $\sim 2.8\ \text{m}\Omega$.

The defect density in the I-a-Si:H layer, as extracted from modeling, is 9×10^{16} cm^{-3} and the Urbach energy is 70 meV (Table III). Schmidt *et al.*[30] have inferred using different characterization techniques (photoelectron spectroscopy, surface photovoltage, and photoluminescence spectra measurements), that for a 10 nm thick I-a-Si:H layer deposited on c-Si(P), good surface passivation could be obtained when the Urbach energy of this I-layer is between 55 and 70 meV and its defect density is $\sim 2\times10^{18}$ cm^{-2}. The Urbach energy used in the present simulations for the I-a-Si:H layer is 70 meV, in good agreement with their work, while the defect density used here is more than an order of magnitude lower. We will show in Sec. IV A, how, according to our model, the defect density in this intrinsic layer itself affects solar cell performance. Modeling also indicates that in order to simulate the lower V_{oc}'s of the Taguchi[6] cells "normal" and "half," the defect density on the surface of the c-Si wafer itself in these cases, should be assumed to be higher (Table II). We may justify this fact by assuming that a very thin buffer layer may not be as effective in passivating the defects on the surface of the c-Si wafer as a thicker buffer layer. The defect density on the front face of the c-Si wafer (the surface that faces the emitter layer and the incoming light) has been taken as $\sim 4\times10^{11}$, 1.5×10^{11}, 10^{10}, 10^{10} cm^{-2} respectively for cases half, normal, double, and triple (Table II). Olibet *et al.*[9] have obtained an interface defect density of between of 7×10^{10} cm^{-2}, after thermal annealing, and 1.7×10^{11} cm^{-2}, after 10 h of dark storage in ambient air, for 5 nm I-a-Si:H layers deposited on N-type c-Si wafers. Our simulations of the above Sanyo results indicate 10^{10} cm^{-2} for $\geq$6 nm thick I-layer and 1.5×10^{11} cm^{-2} for a 3 nm thick one.

Coming back to the simulation parameters, another important parameter difference we had to assume in modeling the solar cell output as a function of the thickness of the I-layer is in the carrier mobilities in the I-a-Si:H layer itself. Due to the very considerable difference in the carrier mobilities between c-Si and a-Si:H, it is likely that the carrier mobilities will reduce more when the amorphous layers are thicker. Anyway, in simulating the considerable fall in the V_{oc} of the cells having the thinner I-a-Si:H layers, half and normal, without increasing the carrier mobilities in the amorphous layers in these cases, we obtained a lower FF than the measured values. It was only when we increased the carrier mobilities in the amorphous front layers (Table II), that the all-round match with experiments was obtained. Increasing carrier mobilities over the front amorphous layers improves hole collection and therefore the FF. Surprisingly it was also

TABLE III. Input parameters used in the modeling of the P-a-Si:H/N-c-Si HJ solar cell normal. The defect density (DL) on the surface of the c-Si wafer, facing the emitter layer is $\sim 1.5\times10^{11}$ cm^{-2} and $\sim10^{10}$ cm^{-2} on the other surface, the front contact barrier height is 1.24 eV, the back contact one is 0.2 eV, and the surface band bending at the front and back contacts are 0.21 and 0 eV, respectively.

Parameters	P a-Si:H	I-a Si:H (buffer)	DL on c-Si (P-side)	N c-Si wafer	DL on c-Si (N-side)	BSF N-a-Si:H
Layer thickness (μm)	0.0065	0.003	0.003	220	0.003	0.02
Mobility gap (eV)	1.75	1.75	1.12	1.12	1.12	1.8
ΔE_v with respect to c-Si (eV)	−0.41	−0.41	0	0	0	−0.46
Donor (Accep) doping (cm^{-3})	(1.41×10^{19})	0	2×10^{15}	2×10^{15}	2×10^{15}	1.45×10^{19}
Effective DOS in CB (cm^{-3})	2×10^{20}	2×10^{20}	2.80×10^{19}	2.80×10^{19}	2.80×10^{19}	2×10^{20}
Effective DOS in VB (cm^{-3})	2×10^{20}	2×10^{20}	1.04×10^{19}	1.04×10^{19}	1.04×10^{19}	2×10^{20}
Charac. energy (VB tail) (eV)	0.05	0.07	⋯	⋯	⋯	0.05
Charac. energy (CB tail) (eV)	0.03	0.04	⋯	⋯	⋯	0.03
Expon. tail prefact. (cm^{-3} eV^{-1})	$4.\times10^{21}$	$4.\times10^{21}$	⋯	⋯	⋯	4×10^{21}
Elec. (hole) mobility (cm^2/V s)	25 (5)	25 (5)	1500 (500)	1500 (500)	1500 (500)	20 (4)
Gaussian defect density (cm^{-3})	9×10^{18}	9×10^{16}	4.5×10^{17}	10^{12}	3×10^{16}	9×10^{18}
Life time of holes (ms) in c-Si				(2.1)		
Neutral σ (tails, midgap-cm^2)	10^{-17}	10^{-14}	10^{-17}	4×10^{-18}	10^{-17}	10^{-17}
Charged σ (tails, midgap-cm^2)	10^{-16}	10^{-12}	10^{-16}	4×10^{-17}	10^{-16}	10^{-16}

found to *decrease* the V_{oc} slightly to enable us to obtain a very good match to experiments (Table II). The reason for the latter is as follows. The conduction band discontinuity being relatively small, some minority carriers (electrons) can rectodiffuse toward the front contact, which is a collector of photogenerated holes. For higher electron mobility, this tendency increases, thus increasing recombination with the photogenerated holes and reducing V_{oc} for the cases having thinner I-layers.

However the main cause of the fall in V_{oc} for thinner I-a-Si:H layers (half and normal) is our assumption of a higher defect density on the surface of the c-Si wafer for these cases. When a P-a-Si:H layer is joined to an N-c-Si wafer, with a high defect density on its surface, most of the electrons that flow from the N-side to the P-side during junction formation, to bring the thermodynamic equilibrium Fermi levels on either side to the same level, leave behind holes that are trapped in the highly defective surface layer of the N-c-Si wafer. The space charge region on the N-c-Si wafer side is therefore localized and does not extend appreciably into the c-Si wafer. We therefore have a higher density of trapped holes on the wafer surface, higher interface field [Fig. 2(a)], and a drop in the field over the adjacent depletion region of the c-Si wafer [Fig. 2(a)—plot of the field on holes as a function of position over the depletion region] for the case with $N_{ss}=4\times10^{11}$ cm^{-2} (case half), relative to the case where this defect density is lower ($N_{ss}=10^{10}$ cm^{-2}—case triple). This results in the observed fall in V_{oc} (Table II). However the FF for cases half and normal remains higher than for cases double and triple, due to (a) thinner I-a-Si:H layers, which have fairly high defect densities and large capture cross sections (Table III) and (b) because of improved carrier collection due to higher carrier mobilities assumed in the thinner I-layers (Table II). Figure 2(b) focuses on the high positive field on the holes at the a-c interface for cases half and triple due to the large valence band discontinuity (ΔE_v), and is given simply for completeness.

The experimental dark current density-voltage characteristics[6] of the cell normal, at different temperatures, is shown in Fig. 1(a) and the model curves in Fig. 1(b). The diode ideality factor, n, calculated in the voltage range $0.4\ V<V<0.8\ V$, from the above model dark characteristics is 1.25. The experimental value (Taguchi *et al.*[6]) is 1.2. This value of "n" indicates that it is the diffusion current that mainly dominates the transport in this voltage range for these N-c-Si HIT cells, as is also the case for homojunction c-Si cells. On the other hand, in the voltage range $0.1\ V<V$

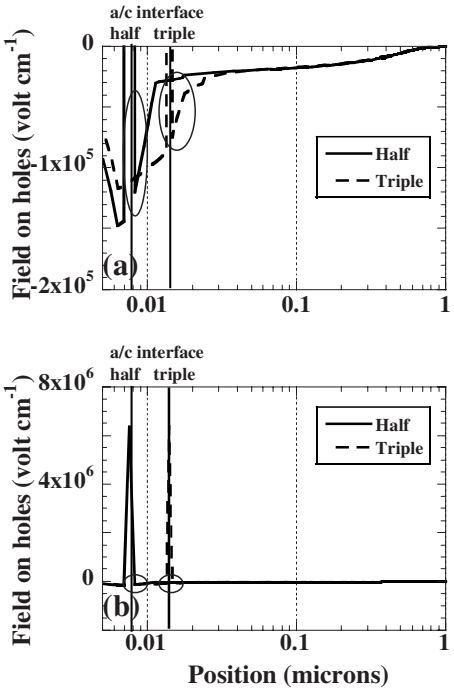

FIG. 2. The electric field on the holes over the depletion region in cells half and triple under AM1.5 illumination and 0 V, (a) focusing on the negative field on the c-Si side and (b) on the large positive field at the a-c interface due to the valence band discontinuity. The encircled portions in the two figures correspond.

<0.4 V, the ideality factor calculated from the modeling data [Fig. 1(b)] lies between 1.006 and 1.05, which indicates that the conductivity continues to be dominated by diffusion. The value of the slope, calculated from the experimental curves of Taguchi *et al.*[6] in the voltage range $0.1\ V<V<0.4$ V, is smaller than that of the recombination current model and remained almost constant for each temperature. The corresponding value of n measured by Taguchi *et al.*[6] is greater than 2^6 [Fig. 1(a)]. Taguchi *et al.*[6] therefore assumed that this is tunneling-limited current. If the value of n, extracted from the experimental curves, had been due to current dominated by recombination, ASDMP would also have been able to reproduce this value of n since the recombination current model is included in ASDMP. In fact ASDMP has already been used to successfully model forward and dark reverse bias characteristics of a-Si:H based PIN solar cells, where recombination plays a dominant role.[31] The fact that the value of n calculated from the ASDMP-generated dark J-V curves is ~1, while that from experiments is different, indicates that the current over this region is dominated by a phenomenon *not* taken account of by ASDMP (e.g., tunneling). Over this voltage region, therefore, the current could be dominated by the tunneling of electrons. However, as pointed out by Taguchi *et al.*,[6] "the current density in this region is sufficiently low compared to the levels of short-circuit current density and does not affect the solar cell performance." It appears then that the solar cell performance under AM1 or AM1.5 light is not affected by tunneling of electrons, although this phenomenon probably exists for $V<0.4$ V. This latter might affect cell performance at lower light intensities. So under 1 sun illumination, the holes surmount the positive field barrier at the a-Si/c-Si interface by thermionic emission for the band gap of the amorphous layers assumed (Table III) in cases of Table II to get collected at the front ITO/P contact. Kanevce *et al.*,[16] in their simulation of HIT solar cells, have included the front contact ITO as an N-type semiconductor into their device model and have concluded that tunneling across the junction interfaces, even under 1 sun illumination, is a critical transport mechanism for attaining efficiencies greater than 20% in HIT cells on N-type c-Si wafers. But the experimental results of Taguchi *et al.*,[6] who have attained efficiencies greater than 20%, indicate that tunneling exists over a range of bias voltage that is unlikely to significantly affect solar cell performance at its normal working condition, as discussed above.

Also, it is possible that the intrinsic a-Si:H layer (with a defect density about two orders of magnitude lower than the doped emitter, Table III), besides passivating the defects on the surface of the c-Si wafer, also suppresses multistep tunneling of electrons from the conduction band of c-Si via the localized states in the I-layer and their ultimate recombination with a hole in the valence band of the a-Si:H (P) layer. Anyway, the defect density in this I-a-Si:H layer needs to be minimized to obtain improved device performance.

The dark forward current always exists even under light and pushes electrons to the front contact and holes to the back, in other words, in a direction opposite to the built-in field. When the applied forward voltage is sufficiently high

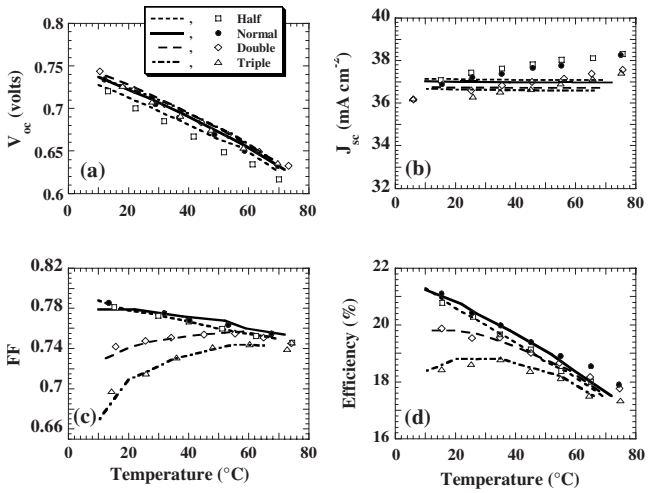

FIG. 3. Variation of (a) V_{oc}, (b) J_{sc}, (c) FF, and (d) Efficiency as a function of temperature in N-c-Si HIT solar cells having different thickness of the undoped a-Si:H layer (half, normal, double, and triple) at the P-a-Si:H/N-c-Si interface. The lines are modeling results, while symbols correspond to measured data.

$(0.4\ V<V<0.8\ V)$, the net electric field inside the device becomes weak and electrons can freely diffuse, therefore they do not *need* to tunnel. The experimental and model dark J-V curve in this voltage region is therefore dominated by diffusion. The diode ideality factor is therefore ~1.2 both from the experimental and model dark J-V curves. However, when the applied forward voltage is *low* $(0.1\ V<V<0.4\ V)$ so that sufficient built-in field remains in the device, specially at the a-c interface, the electrons may move toward the front contact and recombine with a hole in the valence band of the P-emitter by the multistep tunneling route, if the I-a-Si:H layer is sufficiently defective. However, this current level is still too small to affect the light J-V characteristics under 1 sun intensity, as already stated.

Figure 3 shows the temperature dependence of the calculated solar cell output parameters. In Table II, we had made a comparison between experiments and modeling at ambient temperature, before and after taking account of the series resistance of the contacts, measured by Taguchi *et al.*[6] to be 2.8 mΩ for these cells. Since this resistance is independent of temperature, we have made the necessary modifications by taking into account this series resistance in Fig. 3 also and the experimental points (symbols) are plotted on our calculated results (lines).

In general, as the temperature decreases, the carrier density decreases through the temperature dependence of the square of the intrinsic carrier density. It means less carrier recombination and therefore a lower reverse saturation current density, J_0, and higher V_{oc} at lower temperatures, as is seen from Fig. 3(a). However, the lower carrier density at lower temperatures, also means that the cell is now more resistive, resulting in a fall in the FF and therefore of the efficiency for the cells double and triple [Figs. 3(c) and 3(d)], where performance is dominated by the undoped a-Si:H layer. Also, for the value of the band gap assumed for the I-a-Si:H layer (Table III), the holes are able to overcome the positive field barrier at the a-Si/c-Si interface [Fig. 2(b)] by thermionic emission to get collected at the front contact. This

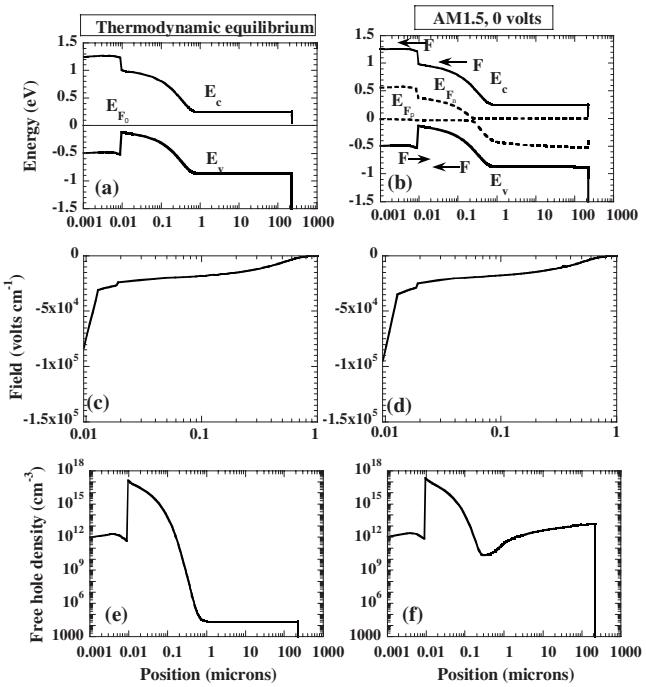

FIG. 4. Calculated energy band diagram, the electric field over the depletion region and the free hole density as a function of position in the device for the case normal in thermodynamic equilibrium [(a), (c) and (e), respectively] and under AM1.5 light in the short-circuit condition [(b), (d), and (f), respectively]. In (b) the electric field (f) on the electrons (in the top part of the figure) and on the holes (bottom part) in the depletion region and at the a-Si/c-Si interface is shown (see text).

thermionic emission decreases at lower temperatures, resulting in a loss of FF for cells double and triple. For cells normal and half having thinner I-layers, the effect of increased resistance at lower temperatures is less marked. Also the positive field on holes at the a-Si/c-Si interface is about 2×10^4 V/cm smaller in half relative to triple, so that the temperature dependence of the thermionic emission also plays a smaller role. Anyway, for these cells normal and half performance is dominated by the temperature-independent resistance of the contacts (Taguchi *et al.*[6]), which has been taken into account also in our calculated results in Fig. 3; therefore, no fall in the FF or efficiency is seen [Figs. 3(c) and 3(d)] for these cases at low temperature. It may also be noted that we did not introduce the temperature dependence of the band gap in these calculations. Therefore our J_{sc} in Fig. 3(b) is constant with temperature, whereas the measured J_{sc} increases slightly with temperature.

IV. SENSITIVITY OF THE SOLAR CELL OUTPUT TO VARIOUS PARAMETERS

The base case for these sensitivity calculations will in general be the model case simulating the experimental case normal (Table II), which shows the highest efficiency. The input parameters for this case are given in Table III. The energy band diagram, the electric field, and the free hole density as a function of position in the device in thermodynamic equilibrium and under AM1.5 light and short-circuit conditions are traced in Fig. 4. We focus on the electric field over the depletion region, as there is no field over the bulk of the absorber (crystalline silicon wafer). The high electric fields at the band discontinuities are not shown here in order to focus on the finer details of the field over the depletion region. According to the sign convention used in ASDMP, negative field is that which pushes holes (electrons) in the negative (positive) x direction and vice versa for the positive field. In the present case, the electric field is negative over the depletion region [Figs. 4(c) and 4(d)], pushing photogenerated holes to the front contact and electrons to the back. Also at the a-Si/c-Si interface, the electric field on electrons is strongly negative [same direction as the field in the depletion layer—shown in the top half of Fig. 4(b)] pushing photogenerated electrons in the c-Si wafer in the right direction (to the back contact); but that on holes is strongly positive, or in the opposite direction to the field in the depletion layer [shown in the bottom half of Fig. 4(b)]. The holes therefore face a strong reverse positive field at the a-Si/c-Si interface [not shown in Fig. 4(d)] due to the a-Si/c-Si valence band discontinuity, whose magnitude relative to the negative field over the depletion region may be estimated by comparing Figs. 2(a) and 2(b). Although a considerable number of photogenerated holes overcome this barrier by thermionic emission and get collected, a large fraction accumulates at and near the a-Si/c-Si interface [Fig. 4(f)], their number depending on the valence band discontinuity. The consequences of this will be dealt with at length, when the sensitivity of the solar cell output to the valence band discontinuity is discussed in Sec. IV C. It may be pointed out that throughout this article (except when the sensitivity to the band gap or the band discontinuity is studied), we have apportioned two-thirds of the band discontinuity at the a-Si/c-Si interface to the valence band edge and the rest to the conduction band edge, as is known to be the case for a-Si:H films deposited by the plasma-enhanced chemical vapor deposition technique.[10,30,32,33] Therefore the positive field barrier at the a-Si/c-Si interface, faced by photogenerated holes that are collected in this structure at the front contact, is larger than that faced by the electrons at the c-Si/amorphous BSF contact in the rear.

A. Sensitivity of the solar cell output to the intrinsic a-Si:H layers on the surface of the c-Si wafer

It is this layer that gives this group of solar cells the name HIT solar cells and is the key to attaining high efficiencies in these structures. In the previous section, we have simulated the solar cell output parameters of N-c-Si HIT cells[6] as a function of the thickness of the intrinsic layer deposited on the front face of the c-Si wafer as well as their temperature dependence. The results have already been discussed in detail and we summarize our findings in this section. The intrinsic layer at the P-a-Si:H /N-c-Si interface influences solar cell performance in three ways: (i) it passivates the defects on the surface of the c-Si wafer[2–4,11,34] which is the reason for its application in the first place; (ii) it reduces the unwanted electron multi-step tunneling to the front contact in the bias voltage range $0.1\ \text{V}<\text{V}<0.4$ V, as well as the beneficial hole tunneling under light, if any, to the front contact; and (iii) reduces the FF of the device if it is thick (Table II) or very defective. Passivation of defects on the front wafer surface improves all aspects of solar cell

TABLE IV. Solar cell output as a function of the defects in the I-a-Si:H layer between the emitter and the N-c-Si wafer.

Defects in I-a-Si:H (cm^{-3})	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	Efficiency (%)
9×10^{14}	36.76	0.718	0.769	20.29
9×10^{15}	36.76	0.718	0.769	20.29
9×10^{16}	36.74	0.717	0.766	20.18
9×10^{17}	36.50	0.707	0.721	18.61

performance, as will be discussed in Sec. IV E. An I-a-Si:H layer is also used to reduce the defects on the rear face of c-Si, but the defects here have a smaller influence on performance (Sec. IV E). Suppression of electron tunneling to the front contact reduces recombination and improves V_{oc}. However, in the event of a fairly wide band gap emitter layer, where the majority carriers, the holes, face difficulty in getting collected and accumulate at the a-Si/c-Si interface, this layer with a defect density at least two orders of magnitude lower than the emitter layer (Table III), suppresses also the beneficial multistep tunneling of holes to the front contact. This will be discussed in more detail in IV C. Finally, it should be kept as thin as possible, without affecting its defect passivation properties, since for thickness greater than ~3 nm, it reduces the FF of the device (Table II).

We now study the sensitivity of the cell output to the defect density of this layer alone assuming a thickness of 6 nm for this I-a-Si:H layer, which is the thickness chosen for the model case that simulates experimental double, and where the best passivation of N_{ss} has already been attained (Table II). Of course increasing the defect density in this layer is still likely to change N_{ss} with strong repercussions on the cell performance, but in the following we assume the latter to be constant. The defects states in this intrinsic layer have high capture cross sections (charged: 10^{-12} cm^2, neutral: 10^{-14} cm^2), as extracted by modeling (Table III). The results are given in Table IV. We find that unless the defect density of the intrinsic layer is $>10^{17}$ cm^{-3}, no significant loss of cell performance occurs. This means that no appreciable improvement of the solar cell efficiencies given in Table II can be achieved by further lowering the defect density in this layer. It may also explain why Schmidt *et al.*,[30] who have achieved a defect density of $\sim2\times10^{18}$ cm^{-3} in their I-a-Si:H layer at the front a-c interface and a P-a-Si:H/N-c-Si HIT cell conversion efficiency of 19.8%, have not been able to equal the higher-than-20%-efficiency of the Sanyo cells.[6]

B. Sensitivity to the P-layer thickness

The results shown in Table V indicate that there is very little fall in the solar cell efficiency even for considerably thick P-layers, though the maximum is at a thickness of ~15 nm. The open-circuit voltage increases up to a thickness of 20 nm, due to an increase of the built-in potential. This is because we have assumed a surface band bending 0.21 eV at the TCO/P interface, so that for very thin P-layers, the activation energy of the bulk P-layer is not attained in the device. However, the fall in efficiency is small since the current decreases slowly. In fact, the decrease is about 1.5 mA cm^{-2}, as the emitter thickness increases from 6.5 to 30 nm.

From the optical point of view, the P-layer should be as thin as possible since the light absorbed in this very defective layer (DL) does not contribute to electrical power. We also find that J_{sc} increases as the P-layer thickness decreases up to 6.5 nm and is in agreement with the findings of other groups, e.g., Refs. 3 and 34. However, for even thinner P-layers (e.g., thickness 5 nm), we get a slight fall in J_{sc}, while Tanaka *et al.*[3] obtained saturation. This is probably due to the low built-in field in the device under this condition that begins to affect carrier collection.

C. Sensitivity of the solar cell output to the P-layer band gap, activation energy, and the valence band discontinuity at the a-c interface

Since the above quantities are interlinked, we treat these sensitivity calculations together. Also, as it is obvious from Table V that the bulk activation energy of the P-layer is not attained in the HIT solar cells for the thinner P-layers, for a more meaningful sensitivity calculation, we assume a P-layer thickness of 30 nm for the following calculations. All parameters, other than $E_{\mu}(P)$, P-layer activation energy (E_{ac}) and ΔE_v are as given in Table III and the I-a-Si:H layer at the P-a-Si:H/N-c-Si interface retains a thickness of 3 nm. The conduction band offset (ΔE_c) is held constant at 0.22 eV. The results are given in Table VI.

The table indicates that for valence band offsets up to 0.51 eV, and $E_{ac}(P)\leq0.3$ eV, the FF is quite high, indicating that the majority of the holes photogenerated inside the c-Si wafer, can surmount the positive field barrier due to the a-Si/c-Si valence band discontinuity by thermionic emission and get collected at the front ITO/P-a-Si:H contact. However, solar cell performance deteriorates both with increasing E_{ac} and band gap of the P-layer. The former is only to be ex-

TABLE V. Variation of the solar cell output with the thickness of the P-layer.

P-a-Si:H thickness (nm)	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	Efficiency (%)	V_{bi} (V)
5.0	36.48	0.704	0.797	20.47	1.106
6.5	37.00	0.712	0.799	21.05	1.125
10	36.68	0.722	0.799	21.16	1.143
15	36.30	0.727	0.809	21.34	1.196
20	36.03	0.728	0.813	21.32	1.225
25	35.75	0.729	0.813	21.19	1.252
30	35.58	0.729	0.810	21.01	1.269

TABLE VI. Variation of the solar cell output parameters with the mobility gap (E_μ), the activation energy (E_{ac}) of the P-layer, and the valence band discontinuity ΔE_v at the P-a-Si:H/N-c-Si interface, in double N-c-Si solar cells. ΔE_c is held constant at 0.22 eV. The P-layer thickness is 30 nm.

E_μ (P) (eV)	E_{ac} (eV)	ΔE_v (eV)	J_{sc} (mA/cm^2)	V_{oc} (V)	FF	η (%)
1.75	0.3	0.41	35.61	0.729	0.810	21.03
1.75	0.4	0.41	35.50	0.717	0.742	18.89
1.80	0.3	0.46	35.78	0.738	0.801	21.15
1.85	0.3	0.51	35.96	0.743	0.758	20.25
1.90	0.3	0.56	36.13	0.750	0.602	16.31
1.90	0.4	0.56	36.05	0.739	0.535	14.25
1.98	0.4	0.64	26.98	0.776	0.176	3.68

pected as it reduces the built-in potential. Figure 5(a) shows the effect on the light J-V characteristics and Fig. 5(b) on the energy band diagram of increasing the P-layer band gap (therefore of increasing ΔE_v, since ΔE_c is held constant) and activation energy. We find that the light J-V characteristics begin to develop an S-shape for higher ΔE_v and E_{ac} of the P-layer. Increasing ΔE_v at the P-a-Si:H/N-c-Si interface results in hole accumulation and therefore a fall in FF for $\Delta E_v \geq 0.56$ eV, for a P-layer activation energy of ~0.3 eV, due to the reverse field it generates; that is further accentuated when E_{ac} is high (Table VI). van Cleef *et al.*[35] have also shown that for a P-layer doping density of 9×10^{18} cm^{-3} (same as ours, Table III, giving $E_{ac}=0.3$ eV) and for $\Delta E_v = 0.43$ eV, normal J-V characteristics are achieved at room temperature and AM1.5 illumination, and that "S-shaped" characteristics begin to develop at higher ΔE_v and E_{ac}. In our case, for $\Delta E_v \geq 0.60$ eV, Fig. 5(c) indicates that free holes accumulate over the entire c-Si wafer, resulting in a sharp reduction of the electric field and flat bands over the depletion region, on the side of the N-type c-Si wafer [Fig. 5(b)]. This fact results in a sharp fall in the FF and conversion efficiency (Table VI). In fact, under this condition, the strong accumulation of holes on c-Si, can partially deplete even the highly defective P-layer, resulting in a shift of the depletion region from c-Si to the amorphous emitter layer [Fig. 5(b)]. This also means that the carriers can no longer be fully extracted at 0 V, resulting in a fall in J_{sc} [Table VI and Fig. 5(a)] and the current recovers to the normal value of ~36 mA cm^{-2} only at a reverse bias [Fig. 5(a)]. Modeling indicates that for improved performance of N-c-Si HIT cells, the valence band offset has to be reduced by a lower emitter band gap, unless the tunneling of holes takes place. Assuming that tunneling does not affect solar cell performance under one sun intensity, unless the band gap of P-a-Si:H ≥ 1.90 eV (for reasons that will be discussed in the following), we agree with the observation of some other researchers[13,14] that the N-c-Si HIT cells having normal band gap P-a-Si:H emitter (E_μ(P) ~ 1.85 eV) are likely to have higher V_{oc}'s (because of a more advantageous band diagram leading to higher V_{bi}), but lower FFs than P-c-Si:H HIT cells, at least the ones with a HJ at the emitter side only[17] due to this hole (majority carrier) accumulation [Fig. 5(c)]. (For the double HIT on P-type c-Si wafer—having HJs at both the emitter an BSF ends—similar hole accumulation occurs at the BSF end of c-Si, reducing its FF.)

We have evaluated the probability of direct tunneling of holes into the P-layer for different valence band discontinuities at the a-c interface using an auxiliary program[28] that has not yet been integrated into ASDMP. We find that the hole direct tunneling current [J_{PDT}(E)] is appreciable for $\Delta E_v \geq 0.60$ eV; therefore, for wide band gap ($E_\mu \geq 1.9$ eV) emitter layers. In Fig. 5(d), we plot the direct tunneling probability [T_p(E)] of holes from the valence band of c-Si to that of a-Si:H, under AM1.5 light and short-circuit conditions for the cell having a valence band offset of 0.64 eV as a function of the hole effective mass (m*), with ΔJ_{PDT}(E) as inset. This quantity is the direct tunneling hole current integrated over a thin but arbitrary constant ΔE interval around each energy E on the potential barrier. The energy, E in Fig. 5(d) is measured from the lower tip of the valence band barrier (ΔE_v) positively upwards. Therefore T_p(E) decreases rapidly with increasing E, while the number of holes in the valence band of c-Si increases. ΔJ_{PDT}(E) therefore passes through a maximum somewhere above the lower tip of the valence band barrier [Fig. 5(d), inset]. T_p(E) and ΔJ_{PDT}(E), as expected, increase with decreasing m*. van Cleef *et al.*[12] have also previously indicated that such tunneling of holes can occur in P-a-SiC:H/N-c-Si HIT cells, for E_μ(p) ~ 2.0 eV. When tunneling occurs, it reduces hole accumulation over the N-c-Si depletion region, improves the field here for cases having high ΔE_v, with consequent improvements in FF and conversion efficiency. Our calculations moreover indicate that such tunneling is not appreciable for $\Delta E_v \leq 0.51$ eV, i.e., for mobility band gaps of the P-layer ≤ 1.85 eV.

Multistep tunneling of holes across the valence band discontinuity is another possibility. Such tunneling may occur if the I-a-Si:H buffer layer between the emitter and the c-Si wafer were defective enough. However, this thin intrinsic layer should have a low defect density to passivate the defects on the front face of the c-Si wafer. Moreover such multistep tunneling is undesirable, even though it can improve the FF, by allowing holes to tunnel through the a-Si/c-Si positive field barrier. This is because if the I-a-Si:H layer were defective enough to allow this, the electrons would also be able to tunnel through to the front contact, increasing recombination with holes over the front amorphous layers, and reducing V_{oc}. It appears therefore that for improved performance of the HIT solar cells on N-type wafers, we should avoid a wide band gap emitter layer. The

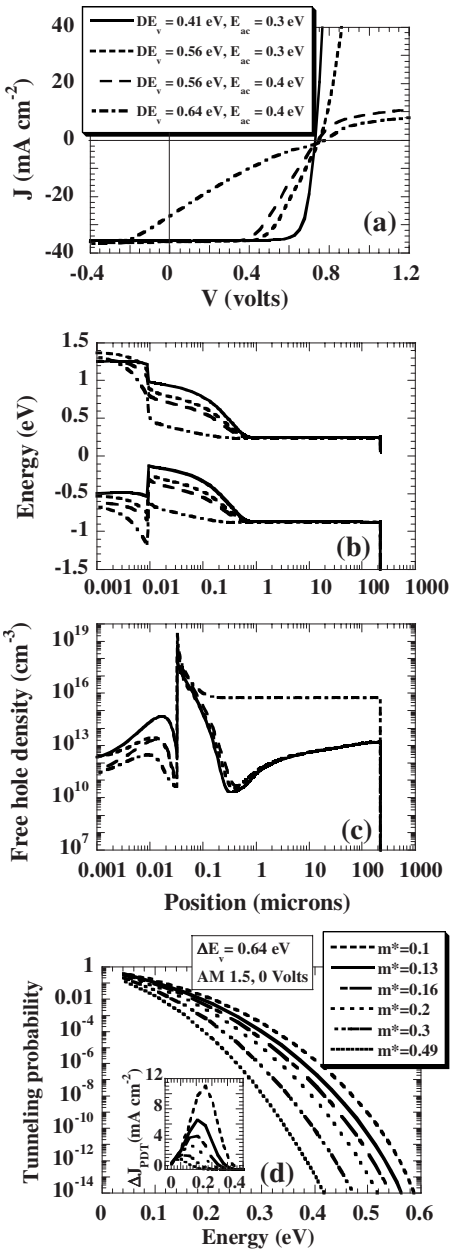

FIG. 5. Variation of (a) the illuminated J-V characteristics, (b) the band diagram under AM1.5 light and 0 V, and (c) the free hole population under the same conditions, as a function of position in the device for different valence band discontinuities (ΔE_v) and activation energies (E_{ac}) of the emitter layer. The legend is the same for figs. (a), (b) and (c). In (d), we plot the direct tunneling probability of holes from the valence band of c-Si to that of a-Si:H for the cell having $E_\mu(p)=1.98$ eV and a valence band offset of 0.64 eV, under AM1.5 light and short-circuit conditions and for different hole effective masses. The energy, E, is measured from the lower tip of the valence band barrier (ΔE_v) positively upwards. The inset to (d) gives the corresponding $\Delta J_{PDT}(E)$ (see text).

most favorable P-layer mobility gap appears to be ≤ 1.85 eV (Table VI) with a reasonable activation energy of 0.3 eV.

In our simulations we have used the classical method (used by most modelers, e.g., Ref. 12) of not including the front contact TCO (here ITO) layer among the semiconductor layers and by treating it therefore as a metallic contact with a high surface recombination velocity at the ITO/P interface and with a reasonably high barrier height. Thus the HIT cell on N-type c-Si wafer is represented as a P/N diode.

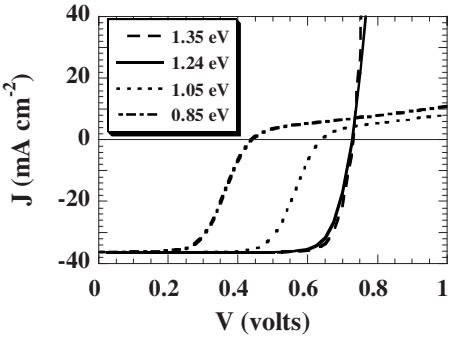

FIG. 6. The current density-voltage characteristics under AM1.5 light and 0 V for different front contact barrier heights. The band gap, the activation energy, and the thickness of the P-layer are held constant at 1.75 eV, 15 nm, and 0.3 eV respectively, so that only surface band bending changes.

Kanevce and Metzger[16] have instead included the ITO layer as a high band gap N-type semiconductor layer and included this in their model treatment. They have then come to the conclusion that tunneling must necessarily take place for N-type c-Si HIT cells to attain efficiencies greater than 20%. However, as already mentioned in Sec. III, the Sanyo cells[6] exhibit efficiencies greater than 20%; yet, the diode ideality factors calculated from the experimental dark J-V characteristics of these cells do not indicate tunneling except in the low bias region, where the current is too small to affect solar cell performance. It therefore appears that a classical treatment of the ITO layer as a metallic contact would suffice to explain N-type HIT cell performance under 1 sun illumination. As already mentioned in Sec. III for performance under lower light intensities, multistep tunneling should be taken into account.

We would like to mention in passing that we have also studied the sensitivity of the solar cell output to the doping density in the N-type c-Si wafer between 5×10^{14} and 10^{16} cm^{-3}. Contrary to the large effect of the a-c interface on the cell performance, there is a very weak sensitivity of the cell output to the doping density in the N-type c-Si wafer.

D. Sensitivity of the solar cell output to the front contact barrier height

The front contact barrier height, ϕ_{b0}, is determined by the following expression:

$$\phi_{b0} = E_\mu(P) - E_{ac}(P) - \text{sbb}, \tag{2}$$

where $E_\mu(P)$ and $E_{ac}(P)$ represent respectively the mobility band gap and the activation energy of the P-layer, and sbb is the surface band bending due to a Schottky barrier at the TCO/P interface. With a change of the work function of the TCO, it is this sbb that varies. In this section, we study the dependence of the solar cell output to changes in this surface band bending. We hold the band gap and the activation energies of the P-layer constant at 1.75 and 0.3 eV, respectively, so that the TCO work function has a direct effect on the front contact barrier height. The results are summarized in Fig. 6. For these sensitivity calculations, we have chosen the thickness of the P-layer to be 15 nm. At this thickness, the activation energy of the P-layer in the device is fairly close to its bulk activation energy, and at the same time it is

TABLE VII. Sensitivity of the solar cell output to the defect density (N_{ss}) in the front and rear surface DLs of the c-Si wafer in N type double HIT solar cells. The P-layer thickness is 6.5 nm. The recombination speeds of holes (S_p—at the front DL) and electrons (S_n—at the rear DL), calculated under AM1.5 light and 0 V, are also shown.

N_{ss} at front (DL) (cm^{-2})	S_p at front (DL) (cm/s)	N_{ss} at back (DL (cm^{-2})	S_n at back (DL) (cm/s)	J_{sc} (mA cm^{-2})	V_{oc} (V)	FF	Efficiency (%)
10^9	3.19			36.96	0.720	0.801	21.32
10^{10}	3.62			36.96	0.720	0.801	21.32
1.5×10^{11}	4.20	10^{10}	2.89×10^4	37.00	0.712	0.799	21.03
10^{12}	24.73			37.24	0.636	0.695	16.46
2×10^{12}	202.62			37.37	0.596	0.470	10.47
10^{13}	1.16×10^3			18.83	0.544	0.160	1.64
		10^9	2.93×10^4	37.00	0.712	0.799	21.03
		10^{10}	2.89×10^4	37.00	0.712	0.799	21.03
1.5×10^{11}	4.20	10^{11}	2.37×10^4	36.99	0.711	0.799	21.01
		10^{12}	1.95×10^4	36.98	0.696	0.797	20.51
		10^{13}	1.00×10^4	35.45	0.609	0.779	16.82

not thick enough to screen the front contact from the rest of the device, in other words, the solar cell output still remains sensitive to the front contact barrier height. Figure 6 indicates that both V_{oc} and FF and therefore the conversion efficiency fall off for $\Phi_{b0} \leq 1.05$ eV.

E. Sensitivity of the solar cell output to the defect density on the front and rear faces of the N-type c-Si wafer

This is shown in Table VII. All aspects of the solar cell output appear to be highly sensitive to the defect density on the front surface (on the side of the emitter layer) of the N-type c-Si wafer for $N_{ss} > 3\times10^{11}$ cm^{-2}; however, the sensitivity to N_{ss} on the rear face is weak and is limited to the condition when these defects are very high. We have also given in Table VII, the values of the corresponding recombination speeds at the a-Si:H /c-Si front and the c-Si/a-Si:H rear HJs, as calculated by ASDMP, under AM1.5 illumination and 0 V. We find that for a well-passivated front interface ($N_{ss} \leq \sim 3\times10^{11}$ cm^{-2}) the recombination speed at this HJ is less than 10 cm/s (Table VII), in good agreement with measured interface recombination speeds.[36]

In Fig. 7(a), we plot the light J-V characteristics and in Fig. 7(b) the band diagram for various values of N_{ss} on the front face of c-Si. We find that for a very high defect density on the surface of the c-Si wafer, the depletion region in the N-c-Si wafer completely vanishes, while the emitter P-layer is depleted [Fig. 7(b)]. With a high N_{ss} on the c-Si wafer, the holes left behind by the electrons flowing into the P-layer during junction formation, are localized on its surface, leading to a high negative field on the wafer surface and little field penetration into its bulk [Fig. 8(a)]. Hence the near absence of the depletion zone in N-c-Si and a strong fall in V_{oc} for the highest N_{ss} (10^{13} cm^{-2}).

In Fig. 8(b), we plot the trapped hole population over the front part and in Fig. 8(c) the electron current over the entire device in N-c-Si double HIT cells under AM1.5 bias light at 0 V. We note that when N_{ss} on the front c-Si wafer surface is the highest (10^{13} cm^{-2}), there is a huge concentration of holes at the crystalline/amorphous interface on the c-Si wafer side, where the high surface defect density exists [dashed line, Fig. 8(b)]. The hole pileup at the crystalline/amorphous interface slows down the arrival of holes to the front contact (the collector of holes), and attracts photogenerated electrons, i.e., encourages their backdiffusion toward the front contact. The result is that the electron current is positive over a considerable part in front of the device [Fig. 8(c)—electron current in the negative x-direction or toward the front contact is positive according to our sign convention]. Thus the electron current collected at the rear contact (the collector of electrons) is lower [Fig. 8(c)] and the backdiffusing electrons recombine with the photogenerated holes over the front part of the absorber c-Si, resulting in poor hole current collection at the front contact also. Thus J_{sc} and FF fall sharply for high values of N_{ss} on the front surface of c-Si (Table VII). In fact, we may arrive at the same conclusion also from Fig. 7(b),

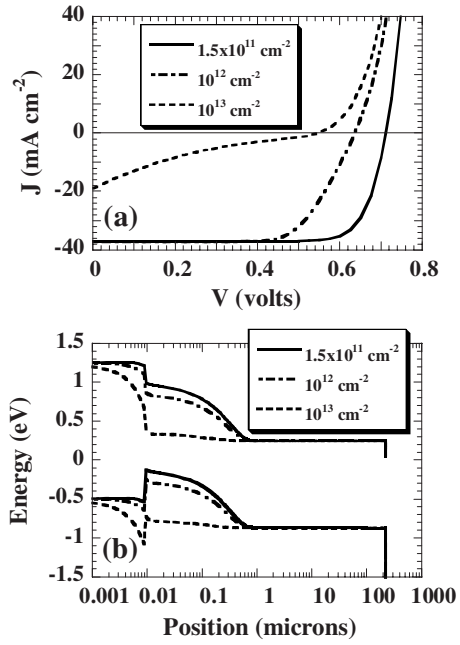

FIG. 7. (a) The light J-V characteristics and (b) the band diagram under AM1.5 light bias under short-circuit conditions for different values of N_{ss} on the front face of the c-Si wafer.

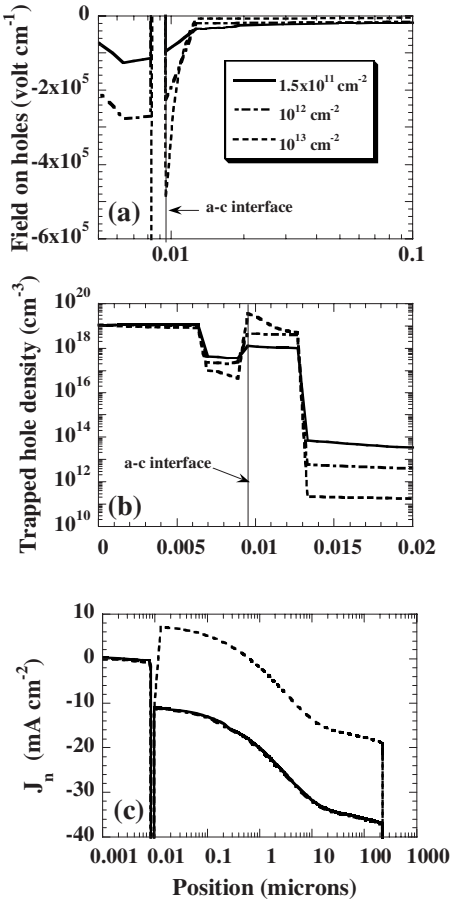

FIG. 8. Plots of (a) the electric field on the holes and (b) the trapped hole density over the front part of the device and (c) the electron current density (J_n) as a function of position in the entire device under illumination and short-circuit conditions, in N-c-Si HIT cells for different densities of defects on the front face of the c-Si wafer. The a-c interface is indicated on (a) and (b).

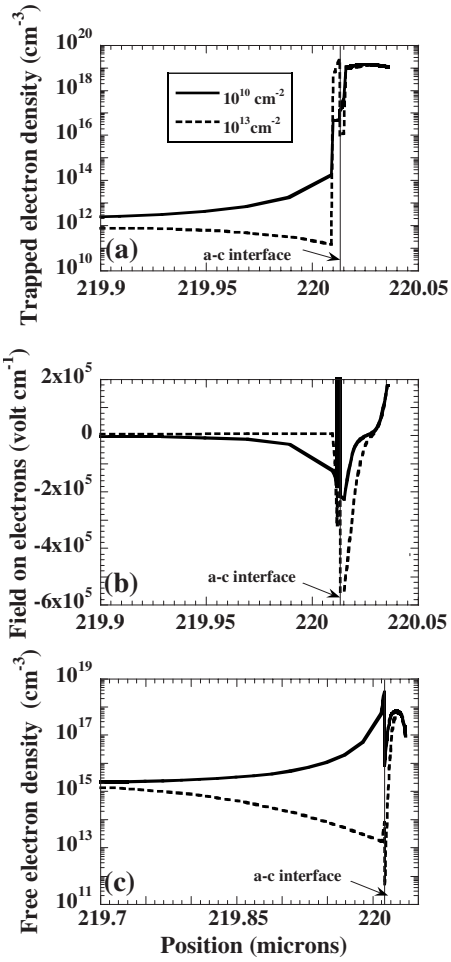

FIG. 9. Plots of (a) the trapped electron density, (b) the field on the electrons and (c) the free electron density over the rear part of the device, under AM1.5 light and 0 V, with the defect density on the rear face of c-Si as a parameter. The a-c rear interface is indicated.

which shows that for $N_{ss}=10^{13}$ cm^{-2}, there is almost no band bending or electric field in the c-Si wafer (the main absorber layer), so that carriers cannot be collected, resulting in the general degradation of all aspects of solar cell performance.

On the other hand, Table VII indicates that there is little sensitivity of the solar cell output to the defect states on the rear face of the wafer, except at the highest value of N_{ss}. Also we note a surprising fact—that the recombination speed through the defect states at the rear face of the c-Si wafer is actually *higher* for a lower defect density. This fact however can be explained with reference to Fig. 9. When the defect density on the rear surface of c-Si is high, the electrons that flow from the highly N-doped a-Si:H BSF layer into c-Si during junction formation, are mainly trapped in these states. Figure 9(a) compares the trapped electron population in the ~3 nm DL at the a-Si/c-Si interface, for cases when N_{ss} on the rear face is low (10^{10} cm^{-2}) and when it is 10^{13} cm^{-2}. For high N_{ss}, the electric field is therefore localized at this a-c interface and does not penetrate into the bulk of c-Si. In fact Fig. 9(b) demonstrates that the field on the electrons toward the rear of the c-Si wafer drops to ~0 beyond the DL for this case, while considerable field exists over the rear part of the c-Si wafer when N_{ss} is low. As a direct consequence, the flux of free electrons arriving at this rear defective surface layer is nearly five orders of magnitude lower for the high N_{ss} case [Fig. 9(c)], resulting in a lower recombination speed at this point, relative to the case having few defects on the wafer surface.

Now to explain the rather low sensitivity of the solar cell output to the rear face N_{ss}, we note that the recombination over the rear region is determined by the number of holes (minority carriers) that can back diffuse to reach the DL. Not many succeed in doing so since the high negative field due to the large valence band discontinuity at the c-Si/a-Si rear interface pushes the holes in the right direction, in other words, toward the front contact. Therefore the defects over this region cannot serve as efficient channels for recombination. Another reason is the fact that the flow of free electrons to the rear contact decreases when N_{ss} is high and vice versa [Fig. 9(c)]; thus, there is no large difference between the recombination through these states for different values of N_{ss} (Table VII). Moreover the conduction band discontinuity at the c-Si/a-Si interface is about half that of the valence band discontinuity. Since the mobility of electrons, relative to that of holes, is also much higher, clearly this reverse field due to the conduction band discontinuity poses little difficulty for

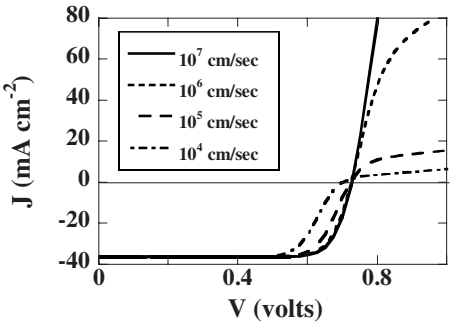

FIG. 10. The sensitivity of the illuminated J-V characteristic under AM1.5 light and short-circuit condition, to the surface recombination speed of the holes at the ITO/P front contact.

electron collection even when the defect density at this point is high, except when $N_{ss} \geq 10^{13}$ cm^{-2}, from which point the solar cell performance deteriorates.

F. Sensitivity of the solar cell output to the surface recombination speeds of the carriers at the contacts

The only surface recombination speed that has a large influence is that of the majority carrier (holes) at the front ITO/P-emitter contact (S_{p0}). The effect of this is shown in Fig. 10, and is seen to lead to S-shaped J-V characteristics with a sharp fall in the FF when reduced to $\leq 10^4$ cm/sec. Holes have a lower mobility than electrons and additionally face a high valence band offset barrier at the a-Si/c-Si interface. Therefore their collection is already somewhat impeded for p-layer mobility gaps ≥ 1.85 eV (Table VI). A low value of S_{p0} can therefore be disastrous for hole collection and the FF of the cell. In fact, when sputtering ITO onto c-Si substrates coated with a-Si:H (intrinsic and doped) films, we sometimes obtain a rather degraded P/ITO interface, where the surface recombination speed is probably reduced. Therefore, Fig. 10 indicates that ITO deposition conditions can also be critical for good solar cell performance.

V. CONCLUSIONS

We have simulated a series of experimental results of the Sanyo HIT cells on N-type c-Si developed over the years, with particular emphasis on the intrinsic a-Si:H layer at the emitter/N-c-Si interface and the temperature dependence of the dark and illuminated J-V characteristics. The simulations were carried out using the electrical-optical model ASDMP, which does not take account of tunneling. We find, that the major breakthroughs in improving the performance of these cells having textured c-Si substrates, come from the introduction of an amorphous BSF layer, by passivating the defects on the c-Si wafer face contacting with the emitter P-a-Si:H and (to a lesser extent) by improving the lifetime of the minority carriers in the c-Si wafer (Table I). Simulations also lead us to conclude that under standard AM1.5 illumination, it is the diffusion current that dominates the performance of HIT solar cells, similar to conventional P/N homojunction cells, and that tunneling is not required to describe the performance of state-of-the-art devices. Moreover estimates with an auxiliary program indicate that the beneficial direct tunneling of holes to the front contact across the valence band offset barrier, has negligible influence for mobility band gaps ≤ 1.85 eV and therefore should not affect cell performance for low to normal band gap a-Si:H emitters and intrinsic layers. Multi-step tunneling of holes to the front contact may still be possible; however we have shown that even without this transport mechanism, the high FFs of the Sanyo cells may be reproduced up to emitter mobility gaps of 1.85 eV, provided its activation energy is ≤ 0.3 eV (Table VI).

Using parameters extracted from modeling, we have calculated the sensitivity of the solar cell output to various material and device parameters. We find that solar cell output is particularly sensitive to the defect states on the surface of the c-Si wafer facing the emitter, to the ITO/P-a-Si:H front contact barrier height and to the band gap and activation energy of the P-a-Si:H emitter, while the I-a-Si:H layer is necessary to achieve both high V_{oc} and FF, as it passivates the defects on the surface of the c-Si wafer (Table VII).

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